REMARKS

Applicant hereby submits this Amendment A, responsive to the Non-final Office Action, Paper No. 1—Date Mailed: August 10, 2005, for which a response is due November 10, 2005 by a shortened statutory period for reply set to expire three [3] months from the mailing date of the Office Action.

Claims 1-48 are pending in the application. Claims 1-19 and 23-48 are rejected. Claims 20-22 are objected to. Claims 1, 7, 20, 28, 36, 37, 41 and 46 are hereby amended. Claims 2-6, 8-19, 21-27, 29-35, 38-40, 42-45, 47 and 48 are original.

Examiner states that Claims 1-10, 12-28, 23-43 and 44-48 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shipley (U.S. 5,633,742) in view of Potash et al. (U.S. 4,893,318) in further view of Brown et al. (U.S. 5,896,380).

Applicants respectfully submit that rejections based upon the combination of Shipley, Potash, Brown and all other art of record are improper and without merit. None of these references teach, suggest, imply or infer combination with one another in order to make such extreme modifications as would be required to exemplify Applicants' claimed invention. It would not have been obvious to one of ordinary skill in the art to make such technical leaps.

Shipley discloses a transmitter responsive to time, divided into time-frames. Shipley states:

> It can be seen that the first time slot in each frame is used as a frame delimiter and never contains an infrared pulse. In FIG. 10, the delimiter time slot is labelled "x". No pulse is allowed to be present in this delimiter time slot. This restriction guarantees that there will always be at least one empty time slot between two consecutive infrared pulses. Seven frames encoding three bits provides a total of 21 bits of data. The 21 bits is comprised of a 16-bit transmitter identity code, a 1-bit low battery or special function code, a 1-bit indicating the programmed transmit interval for the transmitter, and a 3-bit code determined by the status of transmitter push button switches 87, 88 and 89 which are activated. (Shipley: (U.S. 5,633,742): col. 17, lines 33-45)

Shipley teaches that time can be divided in time frames, and that delimiters can be used between data belonging to different time frames. Shipley teaches how to use timing signals for transmission between the fabrics. Shipley states:

> FIGS. 12A, 12B and 12C show how each time slot is divided into three legal pulse position areas, "e" (early), "-"(centered) and "1" (late), plus one illegal area "b" bridging two time slots. If any of the seven subsequent pulses is received earlier than it should arrive as shown in FIG. 12A, the receiver clock time is adjusted back by one position so that the next pulse will be received in the center of the time slot and will be accepted. A pulse which is received in the "late" position causes the receiver to adjust its time clock back one position and will be initially rejected as shown in FIG. 12B. Similarly as shown in FIG. 12B, if a pulse is found to be between or bridging two time slots, the packet is rejected. Similarly if a pulse 196 is found in the frame delimiter time slot as shown in FIG. 12C, the packet is rejected. (Shipley (U.S. 5,633,742): col. 18, lines 38-52)

> In step 304 as discussed above if there is a pulse in the frame delimiter slot, as illustrated in FIG. 12C, the entire packet is rejected, as indicated in step 305. The next check step 306, is whether there is a pulse in or between two time slots; in other words, when a pulse is bridging two slots, the entire packet is rejected (see FIG. 12B). (Shipley (U.S. 5,633,742): col. 19, lines 32-37)

Shipley, alone or combined with any other reference of record, does not teach or suggest how solve the problems arising from cells coming from different inlet fabrics not being aligned when they arrive to the core fabric and cells arriving to the outlet fabric not being aligned when they arrive from different core fabrics as does Applicants' claimed invention. Such misalignment occurs when cells travel for a distance from one fabric to the next. In Shipley, scheduling the queuing of data within a core fabric (memory) is based upon time intervals, and not upon a common time reference as in Applicants' claimed invention. Shipley states:

> Each receiver 24 also includes a timing clock 61 connected to the main processor 51. (Shipley (U.S. 5,633,742): col. 7, lines 30, 31)

> When the transmitter 31 is transmitting automatically and periodically, a slow clock 171 controls the transmit interval rate. The unique identity code of the transmitter 31 and the transmit interval rate can be externally programmed into the identification and rate data register 52 as hereinafter explained. To accommodate the possibility of many thousands of transmitters in a system, it is desirable that the programming for the transmitters 31 be fast and reliable and be accomplished in the manner hereinafter described. (Shipley: (U.S. 5,633,742) col. 8, lines 27-35)

> As shown in FIG. 9, each transmitter 31 is provided with a slow clock 171. The slow clock 171 consists of a 130 Hz resistive-capacitive oscillator which is provided by a transistor Q5 operating in conjunction with integrated circuit U5 which is a 4060-type ripple counter that divides the 130 Hz frequency into

> selectable transmission intervals and multiple repeat message rates. During the normal interval of transmission, the divided down outputs of integrated circuit U5 are applied to the inputs of the integrated circuit U6 of the fast clock enable circuit 161 as shown in FIG. 7. As shown the outputs from the integrated circuit U5 are 8 Hz and 2 Hz and two seconds and eight seconds respectively. The programmed transmit interval data controls whether the eight-second or the two-second interval clock generates the ICLOCK output. (Shipley (U.S. 5,633,742) col. 12, lines 29-43)

Applicants' claims provide for the storing of data based on the delimiter signals and the common time reference. Shipley does not suggest, imply or infer the use of a common time reference. Therefore, Shipley does not teach, suggest, imply or infer Applicants' claimed invention, and Applicants respectfully submit that rejections based upon the combination of Shipley, Potash, Brown and all other art of record are improper and without merit.

Potash simply teaches how to build a common time reference. Shipley states:

> A master (virtual) clock is situated at a central data gathering station, and slave (physical) clocks are situated at one or more (functionally or spatially) remote stations. Time signals are exchanged between the master clock at the central station and each slave clock at each corresponding remote station. From these signals (i) the ratio between the frequencies of the central station master clock and the corresponding remote station slave clock is determined, (ii) the difference in reference (starting) time value between the central station master clock and the corresponding remote station slave clock is determined, and (iii) the transmission time between the central station master clock and the corresponding remote station slave clock is determined. Averages of the clock ratio, reference time, and transmission time are determined across successive time signals to provide improved accuracy. The clock ratio and reference time values are used to derive data referenced to the master clock at the central station from data collected via the slave clock at the remote stations so that the time and data values associated with the data correspond to time and data values generated by the master clock at the central station. If desired, a (virtual) master clock can be determined having time values which are the average of the master clock and all slave clock time values. (Potash et al. (U.S. 4,893,318): Abstract)

Potash does not, in any way, teach, suggest, imply or infer Applicants' claimed invention. Potash and Shipley do not teach, suggest, imply or infer combination with one another in order to make such extreme modifications as would be required to exemplify Applicants' claimed invention. In fact, Examiner admits: "Shipley does not specifically disclose a coordinated universal time signal providing a common time reference; wherein the CTR is coupled to a

transmitter subsystem and a receiver subsystem; wherein the receiver subsystem is responsive to the delimiter signals and the CTR, for storing the received data units from the communications channel. Potash discloses a master clock transmitting timing signals to a number of remote stations containing slave clocks.... The combined teachings of Shipley and Potash do not specifically disclose the receiver subsystem being responsive to the delimiter signals and the CTR, for storing the received data units from the communicated channel." Furthermore, Potash's given time reference does not provide a common time reference utilizing a Coordinated Universal Time (UTC) signal as does Applicants' claimed invention; nor does Potash teach, suggest, imply or infer utilization of UTC.

Brown discloses an ATM switch handling cells after having aligned them to a local clock. Brown states:

> FIG. 7 illustrates the function of an inlet fabric scheduler over a selected interval of sixteen time slots. A maximum of one cell per inlet fabric arrives during a time slot. Here, we observe the traffic destined to a given outlet fabric Y from inlet fabric X. The cell arrival is shown in the top row. The next row shows the number of cells under preparation for transfer to the core during each slot. Once the scheduler decides to transfer a cell group from a queue, the age counter of the queue is reset to zero if the transfer results in an empty queue. Similarly, once the number of waiting cells reaches the full size of a cell group (four in this example) or integer multiples thereof, the age counter is reset to zero. (Brown et al. (U.S. 5,896,380): col. 9, lines 33-47)

Examiner combines the teachings of Shipley, Potash, and Brown in order to invent a scheduler within the receiver, for scheduling the queuing of data within a core fabric (memory) based upon an interval of time, leading to schedule the storing of data based on a given time reference, which is the common time reference built according to Potash's teachings. However, Applicants' claims call for storing of data based on the delimiter signals and the common time reference. This is a fundamental distinction when the core fabric, inlet fabric, and outlet fabric described in Brown's disclosure are physically far from each other.

Brown discloses a system that locally queues cells at a core fabric, wherein cells are coming from an inlet fabric and are subsequently moved to an outlet fabric responsive to a common time signal. Brown creates a fixed channel, or route, between two points whenever data transfer begins. Brown does provide an alignment subsystem responsive to the time frame delimiter, and to the received data units, to store each of the respective received data units

mapped according to the respective one of the time frames associated with the sending of the respective received data units as in Applicants' claimed invention. However, Brown is not analogous to Applicants' claimed invention. Brown states:

> For example, FIG. 3 shows each of cells "A", "B", "C", and "D" in the third queue of each of the core stage fabrics 20-I, 20-II, 20-III, and 20-IV, respectively, and shows each as the third cell in this queue. This result follows from the fact that four cells in a burst are all destined for the same outlet stage fabric and so each will be placed on the queue for that outlet stage fabric in each of the four core stage fabrics. Thus, whenever a cell is added to one particular queue in a core stage fabric, a cell is necessarily added to the corresponding queue of each of the other core stage fabrics. Therefore, corresponding queues in each of the four core stage fabrics are always the same length, with cells at a given rank in the queue all originating from one inlet stage fabric. Put another way, the cells from a burst are all aligned in the core stage.
>
> As described, four cells arrive at the core stage fabric 18 every clock cycle.
>
> Clock 80 is also used to clock cells out of the core stage 18 and into the outlet stage 22. On each cycle of clock 80, the controller 68 of each of the four core stage fabrics 20 transmits one cell from a corresponding one of its eight queues so that four cells are transmitted in one clock cycle all destined for the same outlet stage fabric. The corresponding queues may be chosen without inter-core stage fabric communication because a given queue in a given core stage fabric will always be of the same length as the corresponding queue in each of the other core stage fabrics. One simple implementation is for the core stages to send cells from their queues on a circulating basis, skipping empty queues. (Brown et al. (U.S. 5,896,380) col. 6, lines 27-55)

Furthermore, Examiner admits: "Shipley does not specifically discloses a queue buffer storing respective ones of the data units received during respective ones of the time frames.... The combined teachings of Shipley and Potash do not specifically disclose the data units being forwarded out of the respective ones of the queue buffers responsive to the CTR.... Shipley does not specifically disclose one of the queue buffers being a control queue buffer for storing the control data."

Additionally, none of the art of record teaches, suggests, implies or infers the use of the control information encoded using at least one of a SONET transport overhead and a SONET path overhead, as in Applicants' Claim 24.

Applicants respectfully submit that rejections based upon the combination of Shipley, Potash, Brown and all other art of record is improper, without merit and hereby traversed. None of these references teach, suggest, imply or infer such extreme modifications as would be required for combination with one another in order to exemplify Applicants' claimed invention. It would not have been obvious to one of ordinary skill in the art to make such technical leaps. Applicants respectfully submit that any rejection or objection based upon any combination of the art of record is hereby traversed and overcome.

Examiner states that Claims 11, 19 and 43 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shipley (U.S. 5,633,742) in view of Potash et al. (U.S. 4,893,318) in further view of Brown et al. (U.S. 5,896,380) in further view of Egbert et al. (U.S. 6,091,707).

As previously submitted herein and above, the combination of Shipley, Potash, Brown and all other art of record (including Egbert) are improper and without merit. Claims 11, 19 and 43 are ultimately dependent upon allowable respective independent Claims 1 and 36. Therefore Claims 11, 19 and 43 are also allowable. Furthermore, Applicants respectfully submit that it would not have been obvious to one of ordinary skill in the art to modify the combined teachings of Shipley, Potash and Brown to contain a field within a frame representing a time stamp.

Examiner states that Claims 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Applicants respectfully submit that rejections based upon the combination of Shipley, Potash, Brown, Egbert and all other art of record are improper and without merit. None of these references teach, suggest, imply or infer, alone or in combination with one another, such extreme modifications as would be required to exemplify Applicants' claimed invention. It would not have been obvious to one of ordinary skill in the art to leap to such a combination. Furthermore, *Panduit Corp. v. Dennison Manufacturing Co.*, 810 F.2d 1561, 1 U.S.P.Q.2d 1953 (Fed. Cir. 1987) has shown that elements of separate patents cannot be combined when there is not of such combination anywhere in those patents. Additionally, there is no evidence of motivation to combine Shipley, Potash, Brown, Egbert and any other art of record to reveal Applicants' claimed invention as obvious, because there is no "suggestion, motivation, or teaching in the prior art whereby the person of ordinary skill would have selected the components that the

inventor selected and use them to make the new device." *Golight Inc. v. Wal-Mart Stores Inc.*, 69 U.S.P.Q.2d 1481, 1488 (Fed. Cir. 2002).

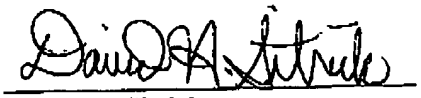
Applicants respectfully submit that any and all bases of rejection or objection are hereby traversed and overcome, and all Claims 1-48 are allowable.

It is respectfully submitted that all bases of rejection of the claims are hereby traversed and overcome, and that the present application be considered in proper condition for allowance. Reconsideration is requested taking the form of a Notice of Allowance or a Notice of Allowability.

No additional fees are due. No new matter has been added. Reconsideration is respectfully requested.

The Examiner is invited to directly communicate with the undersigned, if it will in any way facilitate the prosecution of the application.

Respectfully submitted,



David H. Sitrick
Attorney for Applicant
Registration No. 29,349

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SITRICK & SITRICK
8340 N. Lincoln Ave., Suite 201
Skokie, IL 60077
Telephone Number: (847) 677-4411
Facsimile Number: (847) 677-4656